ANALOG DEVICES

AN-695
APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106 • Tel: 781/329-4700 • Fax: 781/326-8703 • www.analog.com

A High Efficiency TEC Controller Solution

by Troy Murphy and Nobuhiro Matsuzoe

INTRODUCTION

The ADN8831 is a thermoelectric cooler (TEC) controller that provides excellent temperature stability and high efficiency. The device includes the temperature measurement and loop compensation amplifiers, allowing direct interface to a thermistor or resistive temperature device (RTD).

This application note describes how to configure and use the EVAL-ADN8831 board. For exact specifications and internal block diagrams, refer to the ADN8831 data sheet. For the complete demo board schematic, refer to Figure 10.

BOARD DESCRIPTION

The EVAL-ADN8831 board is a complete application circuit for controlling temperature with a TEC. The TEC current is driven using two pairs of complementary MOSFETs in an H-bridge configuration. The demo board provides a simple user interface for temperature and compensation loop gain adjustment. The loop compensation circuit is optimized to work with most telecom cooled laser applications where a 10 kΩ thermistor (3450 β-constant) and TEC are built into the laser module. A green LED illuminates when thermistor temperature is within ±0.1°C of the target temperature.

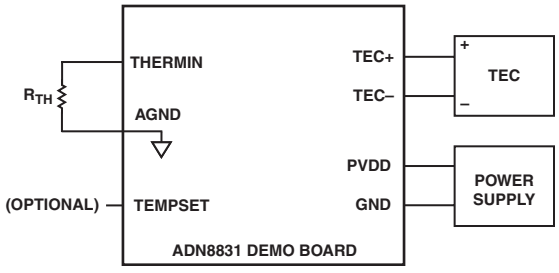

Figure 1. EVAL-ADN8831 Application Block Diagram Getting Started

GETTING STARTED

To ensure proper operation, follow the steps described below. Figure 1 shows the configuration of this setup.

1. Verify the board jumpers are at their default settings:

   JP1—Open. This disconnects the temperature set potentiometer (R19) from the TEMPSET input.

   JP2—Short. This shorts the AGND and PGND planes. A high frequency inductor may be inserted at JP2 to reduce switching noise on AGND, if required.

   JP3—Open. Short this jumper to enable low-current shutdown.

   JP4—Open. Short this jumper to place the ADN8831 in standby. Standby brings the TEC current to 0 A.

2. Connect the thermistor between the board pads labeled THERMIN and AGND. Although any value of thermistor can be used, this board is optimized for best temperature-to-voltage linearity when using a 10 kΩ thermistor at 25°C, β = 3450 thermistor.

3. Connect TEC+ of the thermoelectric cooler to the board pad TEC+, and TEC– to the board pad TEC–.

4. With the power off, solder power supply wires to board pads PVDD and GND. Keep the power supply to this board between 3.0 V and 5.5 V for proper operation.

5. Turn on the power supply. The thermistor temperature locks to approximately 25°C. The green LED illuminates within several seconds, indicating successful temperature lock.

ADJUSTING TEMPERATURE

The voltage at the TEMPSET pad sets the target temperature. The EVAL-ADN8831 board adjusts the TEC current until the voltage at OUT1 equals the voltage at TEMPSET. With nothing connected to the TEMPSET pad

and JP1 opened, R5 and R6 set the TEMPSET voltage to approximately 1.2 V, which corresponds to 25°C.

There are two methods for adjusting the target temperature. 1) Apply a voltage source or DAC directly to the TEMPSET pad, or 2) short JP1 and adjust the R19 potentiometer. With R10 set to 0 Ω, R19 adjusts the temperature value from approximately –6.8°C to +56.8°C.

The input voltage to TEMPSET must be between 0 V and VREF. The voltage-to-temperature sensitivity of the TEMPSET input is determined by the thermistor amplifier gain, which is controlled by the R10 potentiometer. The exact equation for the target temperature (TSET) is

$$T_{SET} = 25°C - m \times (TEMPSET - VREF / 2) \quad (1)$$

where:

VREF is approximately 2.4 V, and

$$m = \frac{40°C}{1\,V} \times \frac{17.68\,k\Omega}{R9 + R10} \quad (2)$$

where *R9* = 17.8 kΩ on the demo board. Note that with R10 set to 0 Ω, a +25.17 mV change in TEMPSET produces a –1°C change in temperature, or a temperature-to-TEMPSET slope of approximately –40°C/V. Setting R10 to 159 kΩ lowers the temperature-to-TEMPSET slope to –4°C/V.

Increasing the value of R10 increases the gain of the thermistor amplifier and reduces the overall target temperature range, but improves the temperature-to-TEMPSET resolution. With R10 set to 0 Ω, a 14-bit DAC is required for TEMPSET to achieve 0.01°C resolution. By setting R10 to 159 kΩ, a 10-bit DAC can be used to get the same resolution. However, the target temperature range is now 21.8°C to 28.2°C.

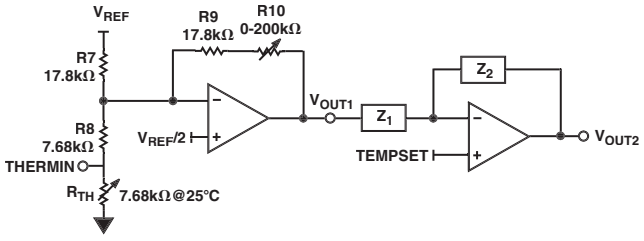

Figure 2. ADN8831 Input and Compensation Amplifier Configurations Temperature Compensation Overview

TEMPERATURE COMPENSATION OVERVIEW

Temperature stability and settling time are determined by the gain and bandwidth of the control loop. This includes the gain of the ADN8831 and the TEC/thermistor feedback. To achieve the highest DC precision, we use an integrator in the loop compensation. Proportional-integral (PI) compensation is preferred because it offers faster setting time over pure integration compensation. The EVAL-ADN8831 is configured for PI compensation.

Settling time is further improved by increasing the overall loop bandwidth. Higher loop bandwidth makes the temperature settle faster to a change in TEMPSET; however, increasing the loop bandwidth past a certain point decreases the phase margin of the loop. Phase margin that is too low causes excessive ringing and steady-state oscillation, or temperature instability.

The bandwidth of the temperature control loop is easily adjusted by increasing the R10 potentiometer. Simply put, increasing R10 improves the temperature settling time for most laser diode applications. However, increasing R10 too high may cause instability.

ADJUSTING TEMPERATURE CONTROL RANGE AND SETTLING TIME

Suggested methods for adjusting the ADN8831 compensation and temperature control range are outlined in this section. Connect a dual trace oscilloscope: one trace monitoring OUT1, the other trace monitoring TEMPSET. Digital scopes are preferred due to the long time constants involved.

You also need to a square wave signal generator to create a step function on the TEMPSET input. This shows the temperature settling time of the loop. Set the square wave amplitude to 100 mV peak-to-peak centered around 1.2 V. Lower the square wave period to 10 seconds; the period may need to be longer for non-laser diode cooling applications.

With the power off, connect the TEC, thermistor, JP1 through JP4 jumpers, and the voltage supply as described in the Getting Started section.

For fixed temperature applications, use the following procedure:

1. Turn R10 clockwise until it is 0 Ω. Do not connect any source to the TEMPSET pad on the board.
2. Activate power. Verify that OUT1 settles to approximately 1.2 V and that the green LED on the board is lit. OUT1 may show some low frequency oscillation on AWG or other non-laser diode applications. If OUT1 is oscillating, increase C10, and verify stability again.
3. Set the temperature by applying the appropriate voltage to TEMPSET from Equation 1.

For applications that require temperature adjustment over a specific range, use this procedure:

1. Calculate R10 according to Equation 2. Record this value as RTEMP. Using an ohmmeter, adjust the R10 potentiometer to that value. Do not connect any source to the TEMPSET pad on the demo board.
2. Activate power. Verify that OUT1 settles to approximately 1.2 V and that the green LED on the board is lit. If OUT1 is oscillating, increase C10 and verify stability again.

3. Connect a square-wave generator to TEMPSET, and monitor the OUT1 settling time with respect to TEMPSET. If the settling time is satisfactory, proceed to Step 8.
4. Adjust R10 for desired settling time response. Generally, increasing R10 (turn the potentiometer counter-clockwise) improves step response speed at the expense of potentially increasing overshoot and ringing.
5. Once R10 is adjusted, turn off the power and measure the resistance of R10 with an ohmmeter. Record this value as R_{CRIT}.
6. Find the required PI compensation according to the Calculating the Ideal Compensation Network section that follows. Adjust the compensation network components to these new values and readjust R10 back to $R_{TEMP.}$ This sets the loop gain for the best settling time with the required R10 value for the desired temperature range.
7. Reactivate the power and the TEMPSET square-wave generator. Monitor OUT1 to verify stability and settling time with the new PI network and R10 value.
8. Set the temperature by applying the appropriate voltage to TEMPSET from Equation 1.

CALCULATING THE IDEAL COMPENSATION NETWORK

The proportional-integral (PI) compensation transfer function is expressed as

$$H(s) = K \times \frac{\left(1+\frac{s}{z}\right)}{s} \quad (3)$$

where *K* is the gain constant and *z* is the zero location of the compensation network. These are given by the equations

$$K = \frac{1}{R11\,C10} \quad (4)$$

$$z = \frac{1}{R16\,C10} \quad (5)$$

The EVAL-ADN8831 board comes with *R11* = 30.1 kΩ, *R16* = 10 kΩ, and *C10* = 10 μF; setting *K* = 10 and *z* = 3.3 rads. Recalculate *K* and *z* if C10 has been adjusted.

The value of R_{CRIT} (found from Step 5 in the previous section) provides the ideal loop-gain for the best settling time. If the value of R_{TEMP} is different from R_{CRIT}, then one needs to adjust the compensation gain *K* to get back to our ideal loop-gain. At the same time, one must keep the compensation zero location at the value of *z*. To do this, set

$$C10 = \frac{1}{K_{NEW}\,R11} \quad (6)$$

$$R16 = \frac{1}{z \times C10} \quad (7)$$

where *z* is found from Equation 8 and

$$K_{NEW} = K \times \frac{R9 + R_{CRIT}}{R9 + R_{TEMP}} \quad (8)$$

with *R9* = 17.8 kΩ and R_{CRIT} and R_{TEMP} recorded from the technique outlined in the Adjusting Temperature Control Range and Settling Time section.

The EVAL-ADN8831 can be reconfigured for PID compensation by adding C8. The desired value for C8 is found experimentally. Although this may improve settling time slightly, PID is much more susceptible to loop instability. PI is generally preferred for most temperature control applications.

Example 1. Our laser diode uses a 10 kΩ at 25°C thermistor. We want to be able to adjust the temperature from 15°C to 35°C. An external DAC will drive TEMPSET. To get the best resolution, we want to use the full DAC output voltage range of 0 V to VREF. Additionally, we want a temperature step response that does not overshoot when settling.

Solution. Connect VREF to the full-scale reference of the external DAC. This ensures that any drift errors on VREF will be common to both the DAC and the thermistor bridge, thus minimizing VREF drift effects. With 25°C centered at 1.2 V on TEMPSET, we need a 1.2 V change in the DAC output to correspond to a 10°C change in temperature. Thus, m = 10°C/1.2 V or 8.333°C/V.

From Equation 2, we calculate R10 = R_{TEMP} = 67 kΩ. We set up the demo board and adjust R10 = 67 kΩ. Examining the settling time of OUT1 (from Step 3), we see some overshoot. We adjust R10 until there is no overshoot and record the value R_{CRIT} = 40 kΩ. From Equation 6 to Equation 8, we set C10 = 4.7 μF and R16 = 64.9 kΩ.

MONITORING TEC VOLTAGE AND CURRENT

VTEC monitors the TEC voltage according to the following equation:

$$VTEC = 0.25 \times (LFB - SFB) + 1.2\ V \quad (9)$$

Output current is sensed by measuring the voltage across the RSN resistor. The voltage across *RSN* is multiplied by 100, offset by 1.2 V, and appears at *ITEC*:

$$ITEC = 100 \times RSN \times (LFB - CSN) + 1.2\ V \quad (10)$$

The ADN8831-EVAL board uses a 10 mΩ sense resistor. This makes the voltage at ITEC increase 1 V for every 1 A of TEC cooling current. Conversely, ITEC decreases 1 V/A with TEC heating current.

The VTEC and ITEC outputs remain active in standby mode, but drop to 0 V in shutdown mode.

SETTING OUTPUT CURRENT LIMITS

The ADN8831 output current protection limit engages when the ITEC voltage falls outside the voltages set at ILIMH and ILIMC. The EVAL-ADN8831 board comes configured with ILIMC tied to VREF (2.4 V) and ILIMH tied to ground through R2 and R22. This provides default heating and cooling current limits of 1.2 A.

To set a higher output current limit, the RSN sense resistor must be reduced. This reduces the sensitivity of ITEC according to Equation 10. For example, set RSN to 5 mΩ to allow ±2.4 A of output current.

Adjust *ILIMC* and *ILIMH* by replacing *R2* and *R22* with appropriate resistors. Their voltages are given as

$$ILIMC = 2.4\ \text{V} \times \frac{R20 + R22}{R2 + R20 + R22} \tag{11}$$

$$ILIMH = 2.4\ \text{V} \times \frac{R22}{R2 + R20 + R22} \tag{12}$$

where *R20* is 19.6 kΩ on the demo board. Solving for *R2* and *R22* in terms of *ILIMC* and *ILIMH* results in

$$R22 = \frac{ILIMH \times R20}{ILIMC - ILIMH} \tag{13}$$

$$R2 = \frac{R20 \times 2.4\ \text{V}}{ILIMC - ILIMH} - R20 - R22 \tag{14}$$

Example 2. The TEC has a heating limit of 0.7 A and a cooling limit of 1.0 A.

Solution. Using the demo board RSN value of 10 mΩ, we calculate ITEC = 2.2 V at 1.0 A of cooling current, and ITEC = 0.5 V at 0.7 A of heating current. Therefore, we need ILIMC = 2.2 V and ILIMH = 0.5 V. We set R22 = 5.76 kΩ and R2 = 2.26 kΩ, which are the closest standard resistor values from solving Equation 14.

Example 3. The TEC has a heating limit of 0.8 A and a cooling limit of 1.8 A.

Solution. Because the current limit exceeds 1.2 A, we must reduce the RSN resistor. Using RSN = 5 mΩ gives an ITEC transfer gain of 0.5 V/A, according to Equation 10. At 1.8 A cooling, ITEC = 2.1 V, and at 0.8 A heating, ITEC = 0.8 V. Therefore, we choose R22 = 12.1 kΩ and R2 = 4.53 kΩ, the closest standard values from solving Equations 13 and 14.

SETTING TEC HEATING AND COOLING OUTPUT VOLTAGE LIMITS

In addition to output current protection, the ADN8831 provides maximum output voltage protection with separate limits for heating and cooling. The maximum output voltage limit is

$$VMAX = 5 \times VLIM \tag{15}$$

Separate heating and cooling voltage limits are achieved through the use of an internal current sink on the VLIM pin as shown in Figure 3. Current source I is 0 A in cooling mode. I increases in heating mode, which lowers the voltage at VLIM according to Equation 17. Thus, the TEC heating voltage limit is always lower than the cooling voltage limit. TECs are much more efficient at heating and generally require a lower maximum heating voltage than cooling voltage.

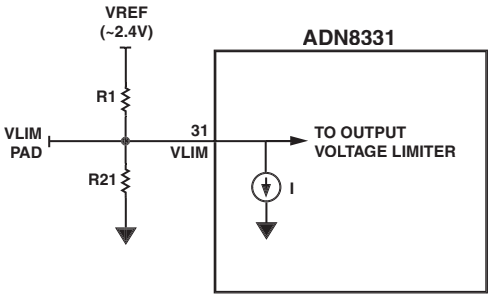

Figure 3. Equivalent Circuit for VLIM Input

The value of I depends on the external resistor value R24 according to Table 1. R24 is also used to set the PWM clock as described in the Adjusting PWM Switching Frequency section. Using resistor divider R1 and R21 on the EVAL-ADN8831 board, the maximum cooling and heating TEC voltages are

$$VLIM_{COOL} = 2.4\ V \times \frac{R21}{R1 + R21} \tag{16}$$

$$VLIM_{HEAT} = VLIM_{COOL} - I \times \left(R21 \| R1\right) \tag{17}$$

The board comes assembled with *R21* = 4.99 kΩ, *R1* = 19.6 kΩ, and RT = 150 kΩ. This sets the TEC heating and cooling voltage limits to 2.24 V and 2.44 V, respectively. To set different output voltage limits, modify R1 and R21 on the demo board. Alternatively, VLIM can be driven directly with a voltage source.

Table 1. VLIM Current and PWM Clock Frequency vs. RT Value

R24	VLIM I-Sink	PWM Clock
150 kΩ	10 μA	1 MHz
300 kΩ	5 μA	500 kHz
500 kΩ	3 μA	300 kHz
750 kΩ	2 μA	200 kHz

Example 4. The TEC is specified for a maximum heating voltage of 2.0 V and a maximum cooling voltage of 2.8 V. We have already selected RT = 150 kΩ in our design.

Solution. From Equation 17, the R21 and R1 resistor divider must set VLIM to 0.56 V when cooling and to 0.4 V when heating. From Equation 17, we see that R1||R21 must equal 16 kΩ. Solving through, we select R21 = 21 kΩ and R1 = 68.1 kΩ.

Example 5. The TEC specifies a maximum voltage of 2.5 V with no distinction between heating and cooling. RT = 300 kΩ in the design.

Solution. We set the heating and cooling voltage limit to 2.5 V. Thus, the parallel resistance of R1 and R21 need to be set to a minimum. For practicality, anything less than 2 kΩ should suffice. Set VLIM to 0.5 V by choosing R21 = 2 kΩ and R1 = 8 kΩ.

STANDBY AND SHUTDOWN MODES

Shorting JP3 puts the ADN8831 into low-current shutdown mode. Shutdown deactivates all ADN8831 circuitry and puts the external FETs into a high impedance state. Open JP3 to reactivate the device.

Standby mode is enabled by shorting JP4. Standby deactivates the output voltage by placing the external FETs into a high impedance state. SYNCOUT is also deactivated; however, VTEC and OUT1 continue to monitor the TEC and thermistor voltages, respectively.

The board continues to draw several milliamps of current in standby mode. Open JP4 to take the ADN8831 out of standby, reactivating the output voltage.

ADJUSTING PWM SWITCHING FREQUENCY

The EVAL-ADN8831 is configured for a free-run PWM clock at 1 MHz. The PWM switching frequency is adjusted by modifying R24 according to Table 1. Reducing the PWM clock slightly improves power efficiency, but increases the output voltage ripple.

BOARD LAYOUT

Figures 4 to 9 show the layout drawings for the silkscreen, top and bottom layers, ground plane, power plane, and drilling guide. These figures are smaller than their actual size.

The power and ground plane drawings are negative masks; they indicate where the solid copper plane is removed. Vias that connect to these planes appear as small, solid circles on the mask. Vias that do not connect appear as larger circles. Via holes are 16 mils with 25 mil isolation pads.

Figure 10 shows the complete demo board schematic for the v1.1 board.

EVAL-ADN8831 V1.1 BOARD LAYOUT DRAWINGS

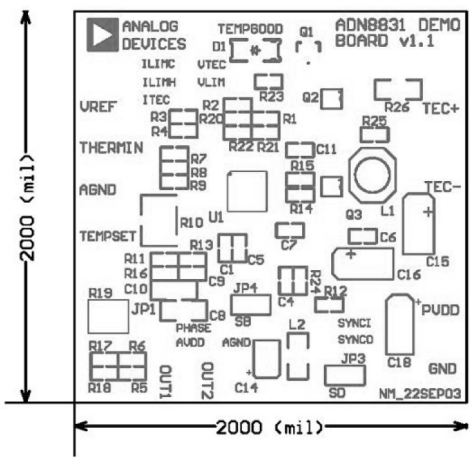

Figure 4. EVAL-ADN8831 v1.1 Top Overlay

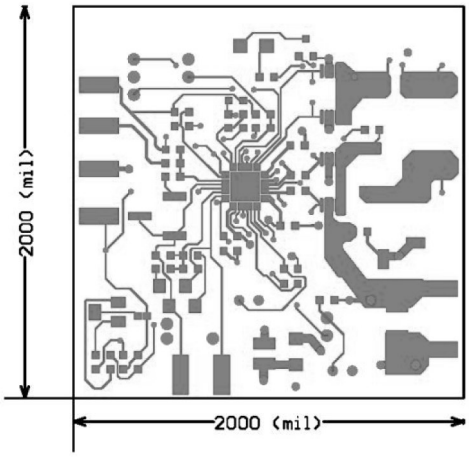

Figure 5. EVAL-ADN8831 v1.1 Top Layer

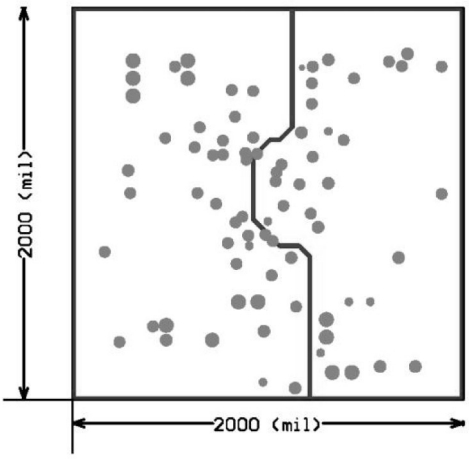

Figure 6. EVAL-ADN8831 v1.1 Power Plane

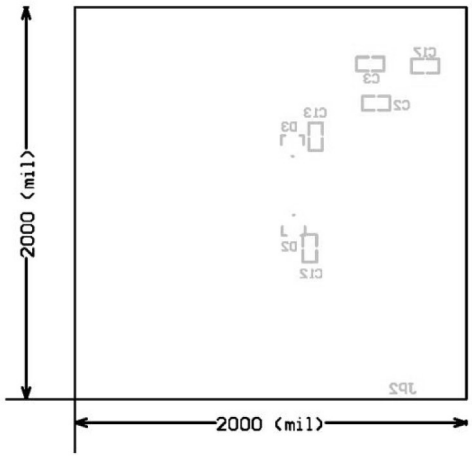

Figure 7. EVAL-ADN8831 v1.1 Bottom Overlay

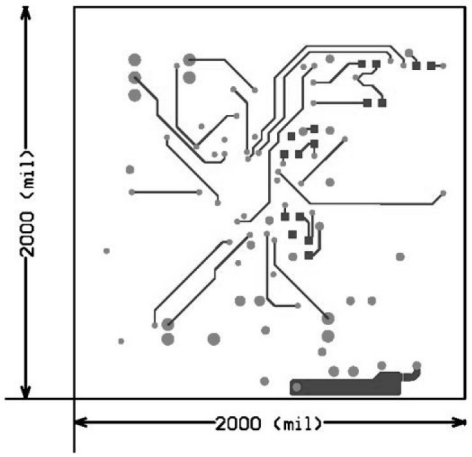

Figure 8. EVAL-ADN8831 v1.1 Bottom Layer

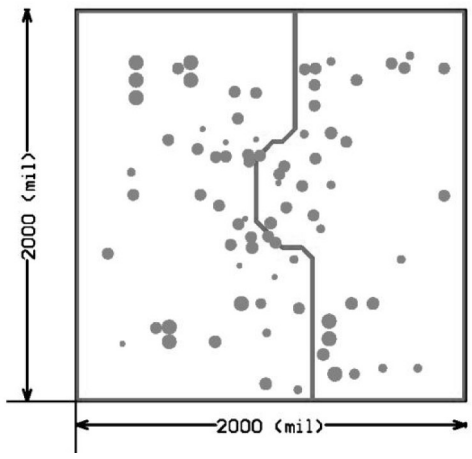

Figure 9. EVAL-ADN8831 v1.1 Ground Plane

DEMO BOARD SCHEMATIC

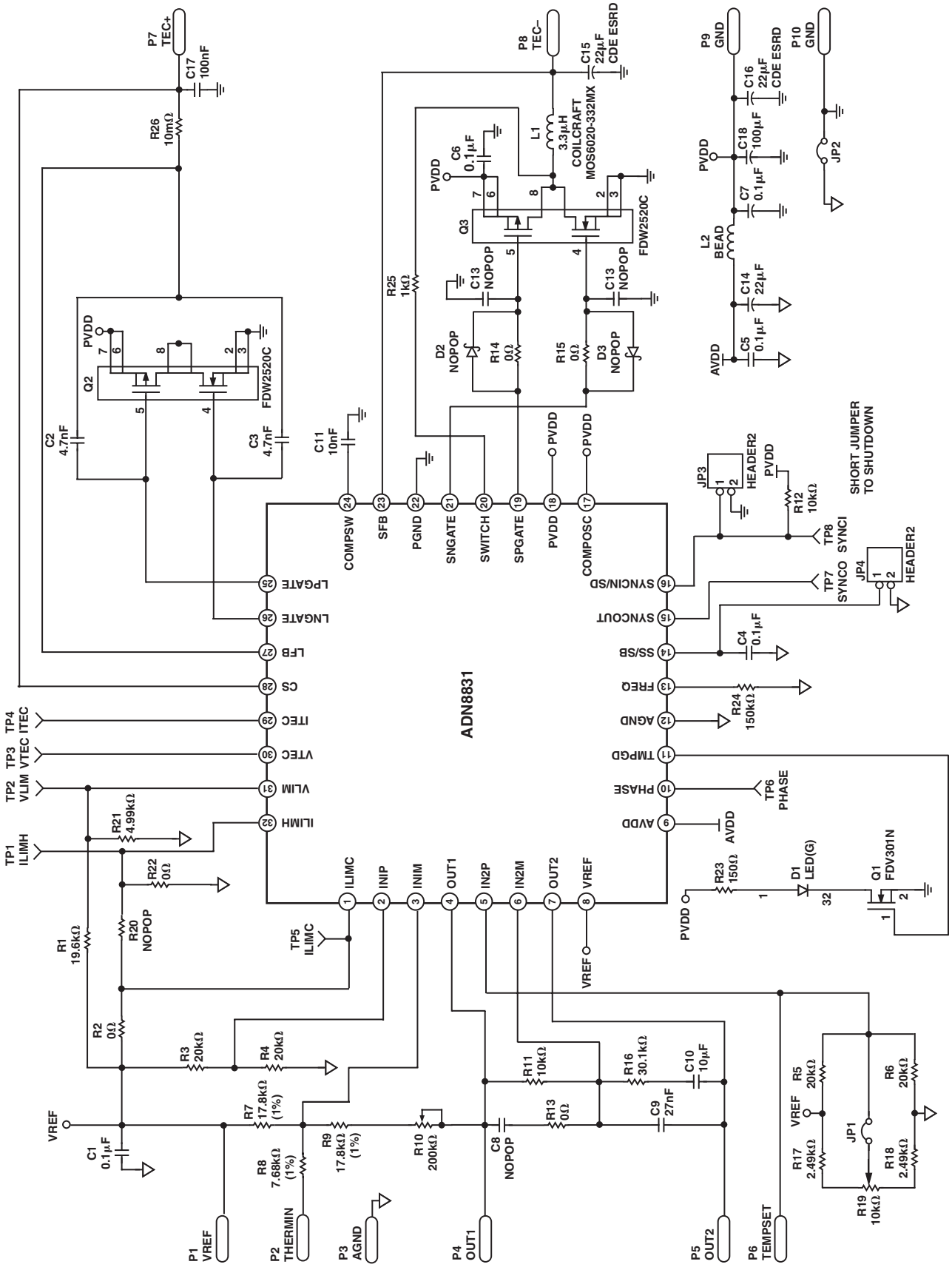

Figure 10. EVAL-ADN8831 Board v1.1 Schematic

AN04592–0–2/04(0)